

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

As rescanning documents *will not* correct images,  
please do not report the images to the  
**Image Problem Mailbox.**

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : **05-102305**  
 (43)Date of publication of application : **23.04.1993**

---

(51)Int.CI. **H01L 21/82**  
**G06F 15/60**  
**H01L 21/3205**

---

(21)Application number : **03-260187** (71)Applicant : **NEC IC MICROCOMPUT SYST LTD**  
 (22)Date of filing : **08.10.1991** (72)Inventor : **SATO AKIHIRO**

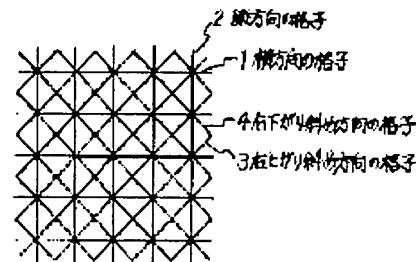
---

**(54) AUTOMATIC LAYOUT METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT**

**(57)Abstract:**

**PURPOSE:** To make the length of wiring short by a method wherein, in addition to wiring layer which is used for wiring on lattices in the transverse and longitudinal directions in conventional cases, a wiring layer which is used for lattice-shaped wiring in the oblique direction is used.

**CONSTITUTION:** In addition to lattices 1 in the transverse direction and lattices 1 in the longitudinal direction, lattices 3 in the rightward ascending oblique direction and lattices 4 in the rightward descending oblique direction are set, they are used as wiring layers which are used mainly for wiring on the respective lattices 1, 2, 3, 4, and a first inter-connection layer to a fourth wiring layer are allotted. Thereby, the length of the wiring can be shortened to 0.7 times at the most, and the wiring resistance and wiring capacitance are reduced. As a result, the operating speed of the title integrated circuit can be made fast.




---

**LEGAL STATUS**

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of

rejection]

[Date of requesting appeal against examiner's  
decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

(19)日本国特許庁 (JP)

(12) 公開特許公報 (A)

(11)特許出願公開番号

特開平5-102305

(43)公開日 平成5年(1993)4月23日

(51)Int.Cl. <sup>5</sup>	識別記号	序内整理番号	F I	技術表示箇所
H 01 L 21/82				
G 06 F 15/60	3 7 0	P 7922-5L		
H 01 L 21/3205				
	9169-4M		H 01 L 21/ 82	W
	9169-4M			C

審査請求 未請求 請求項の数1(全3頁) 最終頁に続く

(21)出願番号 特願平3-260187  
(22)出願日 平成3年(1991)10月8日

(71)出願人 000232036  
日本電気アイシーマイコンシステム株式会社  
神奈川県川崎市中原区小杉町1丁目403番  
53  
(72)発明者 佐藤 昭宏  
神奈川県川崎市中原区小杉町一丁目403番  
53日本電気アイシーマイコンシステム株式会社内  
(74)代理人 弁理士 内原 晋

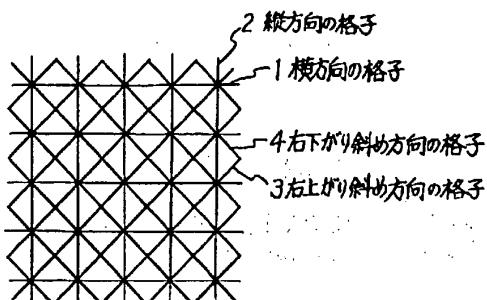
(54)【発明の名称】 半導体集積回路の自動レイアウト方法

(57)【要約】

【目的】 決められた格子の上を定められた配線層で配線するアルゴリズムを用いた半導体集積回路の自動レイアウト方法で配線した配線の長さを短かくする。

【構成】 横方向の格子1および縦方向の格子2に加えて新たに斜め方向の格子3, 4を設け、それぞれの格子上に主に使う配線層を定める。これにより配線すると、A点B点間の配線パターン5、C点D点間の配線パターン6のようになる。

【効果】 配線の長さを最大0.7倍に短かくすることができ、配線抵抗と配線容量が減るので動作速度が速くなる。



1

## 【特許請求の範囲】

【請求項1】少なくともひとつの横方向の格子上の配線に使う配線層と、少なくともひとつの縦方向の格子上の配線に使う配線層と、少なくともひとつの斜め方向の格子上の配線に使う配線層とを用いることを特徴とする半導体集積回路の自動レイアウト方法。

## 【発明の詳細な説明】

## 【0001】

【産業上の利用分野】本発明は半導体集積回路の自動レイアウト方法に関し、特に決められた格子の上を定められた配線層で配線するアルゴリズムを用いた自動レイアウト方法に関する。

## 【0002】

【従来の技術】従来の決められた格子の上を定められた配線層で配線するアルゴリズムを用いた半導体集積回路の自動レイアウト方法は、例えば図3に示すように、第1の配線層を主に横方向の格子11上の配線に使い、第2の配線層を主に縦方向の格子12上の配線に使っていった。さらに、3層以上の配線層を使う場合は、第3の配線層を第1の配線層と同一の横方向の格子11上、第4の配線層を第2の配線層と同一の縦方向の格子12上、というように順次割り当てて使っていった。

【0003】図4は図3の格子に従って実際に配線したパタン図である。図4において、横方向に第1の配線層15があり、縦方向に第2の配線層16があり、各配線層15、16の接続パタン17で電気的に接続されている。これらは、A、B点、C、D点間の電気的接続をするための配線パタンである。

## 【0004】

【発明が解決しようとする課題】このような従来の半導体集積回路の自動レイアウト方法では、たとえ3層以上の配線層を使っても横方向または縦方向の格子11、12上にしか配線しないので、配線層を増やしても配線がしやすくなるだけで、配線の長さはあまり短かくならないという問題点があった。

【0005】本発明の目的は、前記問題点を解決し、配線の長さを短かくする半導体集積回路の自動レイアウト方法を提供することにある。

## 【0006】

【課題を解決するための手段】本発明の半導体集積回路の自動レイアウト方法の構成は、少なくともひとつの横

2

方向の格子上の配線に使う配線層と、少なくともひとつの縦方向の格子上の配線に使う配線層と、少なくともひとつの斜め方向の格子上の配線に使う配線層とを用いることを特徴とする。

## 【0007】

【実施例】図1は本発明の一実施例で使用される配線格子図である。図1において、横方向の格子1と縦方向の格子2に加えて、右上がり斜め方向の格子3と右下がり斜め方向の格子4とを設定し、それぞれの格子1、2、

10 3、4上の配線に主に使う配線層として、第1から第4の配線層を割り当てる。

【0008】図2は図1の格子図を用いて配線パタンを行ったパタン図である。

【0009】図2において、第1の配線層7、第2の配線層8、第3の配線層5、第4の配線層6とがあり、各配線層間の接続パタン9が接続点等に設けられている。

【0010】図2では、A点B点間、およびC点D点間を配線した例で、従来の図4と比べて、配線の長さが0.7～0.8倍に短くなっている。

20 【0011】

【発明の効果】以上説明したように、本発明は、従来の横および縦方向の格子上の配線に使う配線層に加えて、斜め方向の格子上の配線に使う配線層を用いることにより、配線の長さを最大0.7倍に短くすることができ、配線抵抗と配線容量とが減るので、動作速度が速くなるという効果を有する。

## 【図面の簡単な説明】

【図1】本発明の一実施例の半導体集積回路の自動レイアウト方法で使用される配線格子図である。

30 【図2】図1の格子に沿って作成した配線パタン図である。

【図3】従来の自動レイアウト方法で使用される配線格子図である。

【図4】図3の格子に沿って作成した配線パタン図である。

## 【符号の説明】

1, 11 横方向の格子

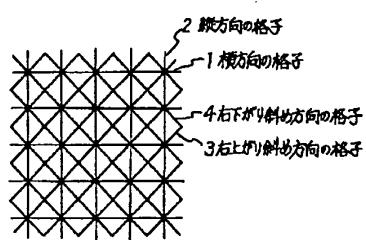
2, 22 縦方向の格子

3 右上がり斜め方向の格子

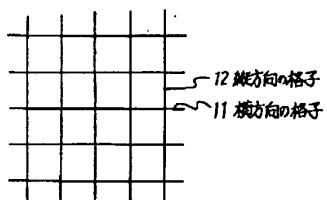
4 右下がり斜め方向の格子

40 5, 6, 15, 16 2点間の配線パタン

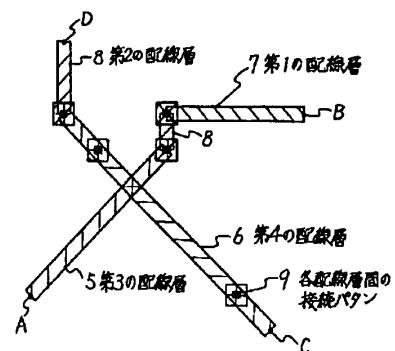
【図1】



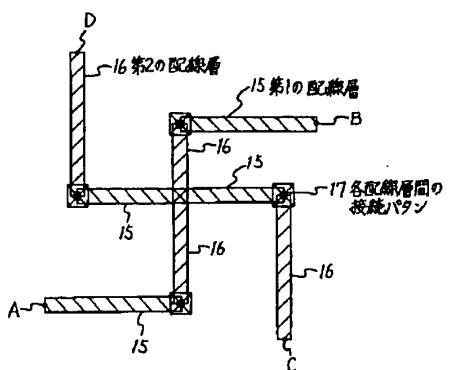
【図3】



【図2】



【図4】



フロントページの続き

(51) Int. Cl. 5

識別記号

府内整理番号

F I

7353-4M

H 0 1 L 21/88

技術表示箇所

A

**(12)UNEXAMINED PATENT APPLICATION GAZETTE (A)**

**(19) Japanese Patent Office (JP)**

**(11) Unexamined Patent Application KOKAI No. H5-102305 [1993]**

**(43) KOKAI Date:** April 23, 1993

---

<b>(51) Int. Cl.<sup>5</sup></b>	<b>I.D. Symbol</b>	<b>Intern. Ref. No.</b>	<b>FI</b>	<b>Tech. Desig.</b>
H 01 L 21/82				
G 06 F 15/60	370 P	7922-5L		
H 01 L 21/3205				
		9169-4M	H01L 21/82	W
		9169-4M		C
		7353-4M	H01L 21/88	A

**Examination Request Status:** Not yet requested

**Number of Claims:** 1      (Total 3 pages [in orig.])

---

<b>(21) Application No.</b>	<b>H3-260187 [1991]</b>
<b>(22) Filing Date:</b>	October 8, 1991
<b>(71) Applicant:</b>	000232036  Nippon Denki Aishimaikon Shisutemu KK  [NEC IC Microcomputer Systems, Ltd.]  1-403-53 Kosugi-cho, Nakahara-ku, Kawasaki-shi, Kanagawa-ken
<b>(72) Inventor:</b>	Akihiro Sato  c/o Nippon Denki Aishimaikon Shisutemu KK

1-403-53 Kosugi-cho, Nakahara-ku, Kawasaki-shi,  
Kanagawa-ken

(74) Agent: Susumu Uchihara, patent attorney

**(54) [Title of Invention]**

**Automatic Layout Method for Semiconductor Integrated Circuits**

**(57) [Abstract]**

**[Purpose]**

To shorten the wiring length of wiring made by an automatic layout method for semiconductor integrated circuits using an algorithm that implements wiring on decided lattice members in determined wiring layers.

**[Constitution]**

In addition to horizontal-direction lattice members 1 and vertical-direction lattice members 2, diagonal lattice members 3 and 4 are newly provided, and the wiring layer primarily used is determined on those lattice members. When wiring is implemented in this manner, the result is a wiring pattern 5 between point A and point B, and a wiring pattern 6 between point C and point D.

**[Benefits]**

It is possible to shorten the wiring length by a maximum factor of 0.7, whereupon wiring resistance and wiring capacitance are reduced so that the operating speed is increased.

**[Claims]**

**[Claim 1]** An automatic layout method for semiconductor integrated circuits that employs a wiring layer using wiring on at least one horizontal-direction lattice member, a wiring layer using wiring on at least one vertical-direction lattice member, and a wiring layer using wiring on at least one diagonal-direction lattice member.

**[Detailed Description of the Invention]**

**[0001]**

**[Field of the Invention]**

This invention concerns an automatic layout method for semiconductor integrated circuits, and more particularly concerns an automatic layout method that uses an algorithm that implements wiring on decided lattice members in determined wiring layers.

**[0002]**

**[Prior Art]**

In a conventional automatic layout method for semiconductor integrated circuits that uses an algorithm that implements wiring on decided lattice members in determined wiring layers, as diagrammed in Fig. 3, for example, a first wiring layer is primarily used in wiring on a horizontal-direction lattice member 11, while a second wiring layer is primarily used in wiring on a vertical-direction lattice member 12. Furthermore, when three or more wiring layers are used, [the additional layers] are allocated in sequence, the third wiring layer being made on the same horizontal-direction lattice member 11 as the first wiring layer, and the fourth wiring layer being made on the same vertical-direction lattice member 12 as the second wiring layer.

**[0003]**

Fig. 4 is a diagram of a pattern actually wired following the lattice diagrammed in Fig. 3. In Fig. 4, there are a first wiring layer 15 in the horizontal direction and a second wiring layer 16 in the vertical direction, with these wiring layers 15 and 16 being electrically connected by a connection pattern 17. These are wiring patterns for making electrical connections between points A and B, and C and D.

**[0004]**

**[Problems Which the Present Invention Attempts to Solve]**

With a conventional automatic layout method for semiconductor integrated circuits such as this, wiring is only implemented on either a horizontal-direction or vertical-direction lattice member 11 or 12, even when using three or more wiring layers. Therefore, even when the number of wiring layers is increased, all that happens is that wiring is made easier, and wiring

length is hardly shortened at all, which constitutes a problem.

[0005]

An object of the present invention is to provide an automatic layout method for semiconductor integrated circuits wherein wiring length is shortened and the problem noted above is resolved.

[0006]

**[Means Used to Solve the Abovementioned Problems]**

The automatic layout method for semiconductor integrated circuits of the present invention is configured so as to employ a wiring layer using wiring on at least one horizontal-direction lattice member, a wiring layer using wiring on at least one vertical-direction lattice member, and a wiring layer using wiring on at least one diagonal-direction lattice member.

[0007]

**[Embodiments]**

Fig. 1 is a diagram of a wiring lattice used in a first embodiment of the present invention. In Fig. 1, in addition to horizontal-direction lattice members 1 and vertical-direction lattice members 2, diagonal-direction lattice members 3 that rise to the right and diagonal-direction lattice members 4 that decline to the right are established, and first, second, third, and fourth wiring layers are allocated as wiring layers used primarily in wiring on lattice members 1, 2, 3, and 4, respectively.

[0008]

Fig. 2 is a pattern diagram wherein a wiring pattern has been made using the lattice diagram of Fig. 1.

[0009]

In Fig. 2, there are a first wiring layer 7, a second wiring layer 8, a third wiring layer 5, and a fourth wiring layer 6, with an inter-wiring-layer connection pattern 9 provided at the connection points, etc.

[0010]

Fig. 2 shows an example of a wiring between point A and point B, and point C and point D. The wiring length is shorten by a factor of 0.7 to 0.8, compared to that of the conventional [wiring] shown in Fig. 4.

[0011]

**[Benefits of the Invention]**

The present invention, as described in the foregoing, by using wiring layers used in wiring on diagonal-direction lattice members in addition to wiring layers used in wiring on the usual horizontal- and vertical-direction lattice members, can shorten wiring lengths by a maximum factor of 0.7, providing the benefits of reduced wiring resistance and wiring capacitance, and faster operating speeds.

**[Brief Description of the Drawings]**

Fig. 1 is a diagram of a wiring lattice used with the automatic layout method for semiconductor integrated circuits in one embodiment of the present invention;

Fig. 2 is a diagram of a wiring pattern produced in conformity with the lattice diagrammed in Fig. 1;

Fig. 3 is a diagram of a wiring lattice used in a conventional automatic layout method; and

Fig. 4 is a diagram of a wiring pattern produced in conformity with the lattice diagrammed in Fig. 3.

**[Explanation of Symbols]**

1, 11 Horizontal-direction lattice members

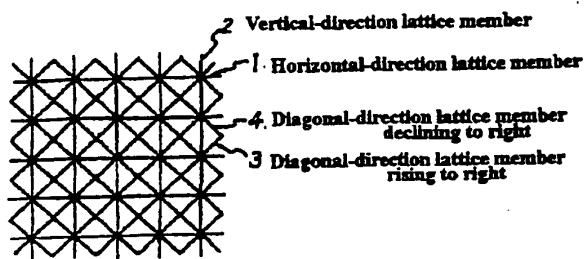
2, 22 Vertical-direction lattice members

3 Diagonal-direction lattice member rising to right

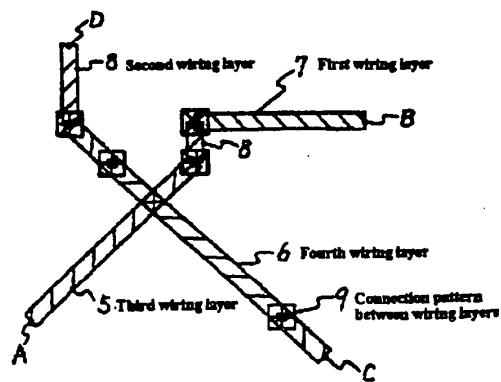
4 Diagonal-direction lattice member declining to right

5, 6, 15, 16 Wiring patterns between two points

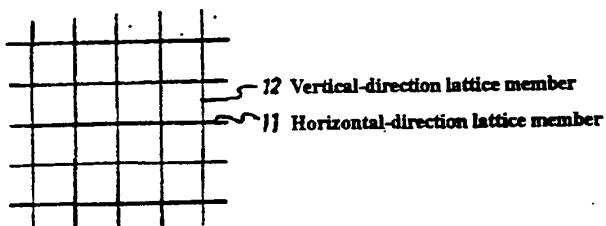
[Figure 1]



[Figure 2]



[Figure 3]



[Figure 4]

